LLC Resonant Half Bridge Converter

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Outline

- Introduction to LLC resonant half bridge converter
    - Benefits
    - Operation principle
    - Design challenges
- Design method
    - Transformer turns ratio selection
    - Magnetizing inductor selection
    - Resonant component selection
- Other design issues for LLC resonant converter
    - Current limiting
    - Soft start
    - OVP and Burst Operation

Design Challenges for DC/DC

- Higher power conversion performance
  - Higher efficiency, smaller heat sink
  - Higher switching frequency, smaller magnetics
  - Less energy storage capacitors, smaller size (e.g., for PFC holdup)
  - Moderate frequency variations

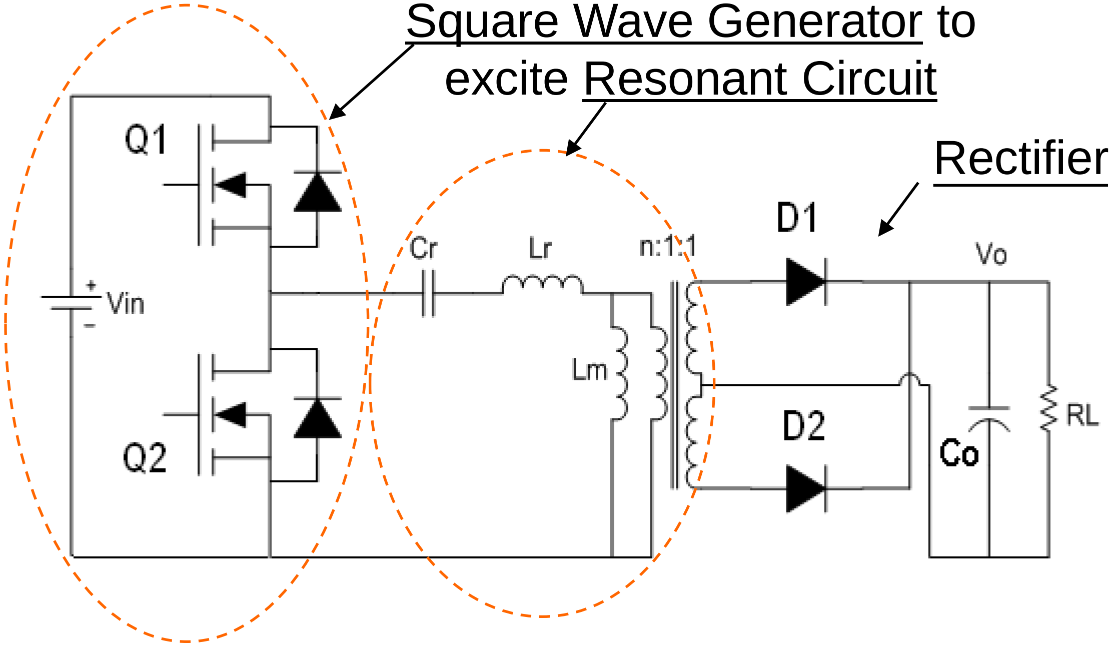
- Wide input voltage variations
  - AC-DC applications: holdup time requirement (PFC from 400V to 300V during holdup)
    - Larger Energy Storage Capacitor – high cost, large size, more space
    - Converter ability to tolerate the variations
  - DC-DC applications
    - Telecom, 36 to 75V (32V to 78V)
    - Some applications even asking 4:1 variations

- Wide output voltage trimming

Benefits of LLC Resonant Converter

- ZVS can be achieved by utilizing transformer magnetizing inductor
- Capacitor filter, less voltage stress on rectifiers
- Smaller switching loss due to small turn off current
- Variable switching frequency control, not sensitive to load change
- Frequency variations can be designed narrower compared to SRC
- Wide operation range without reducing normal operation efficiency

LLC Resonant Converter with Wide Operation Range



Square Wave Generator to excite Resonant Circuit

Rectifier to get DC

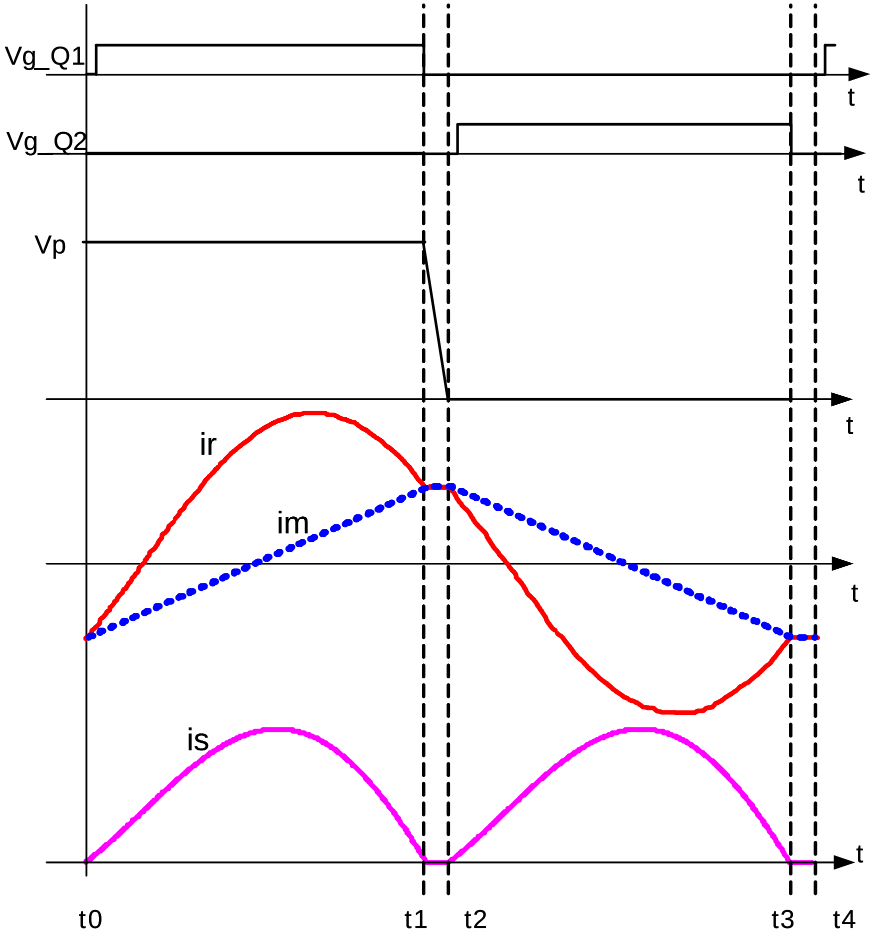
Resonant frequency $f_0 = \dfrac{1}{2\pi\sqrt{L_r C_r}}$

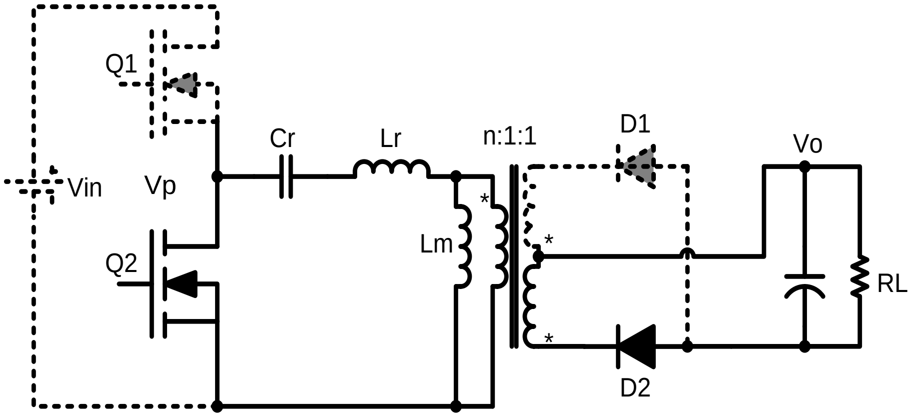
Transformer turns-ratio $n = \dfrac{V_{in}/2}{V_o}$

- f_{sw} **is set at resonant frequency at nominal input and output**
- f_{sw} **is adjusted by feedback loop at other operation conditions**

Operation Principles

At Resonant Frequency

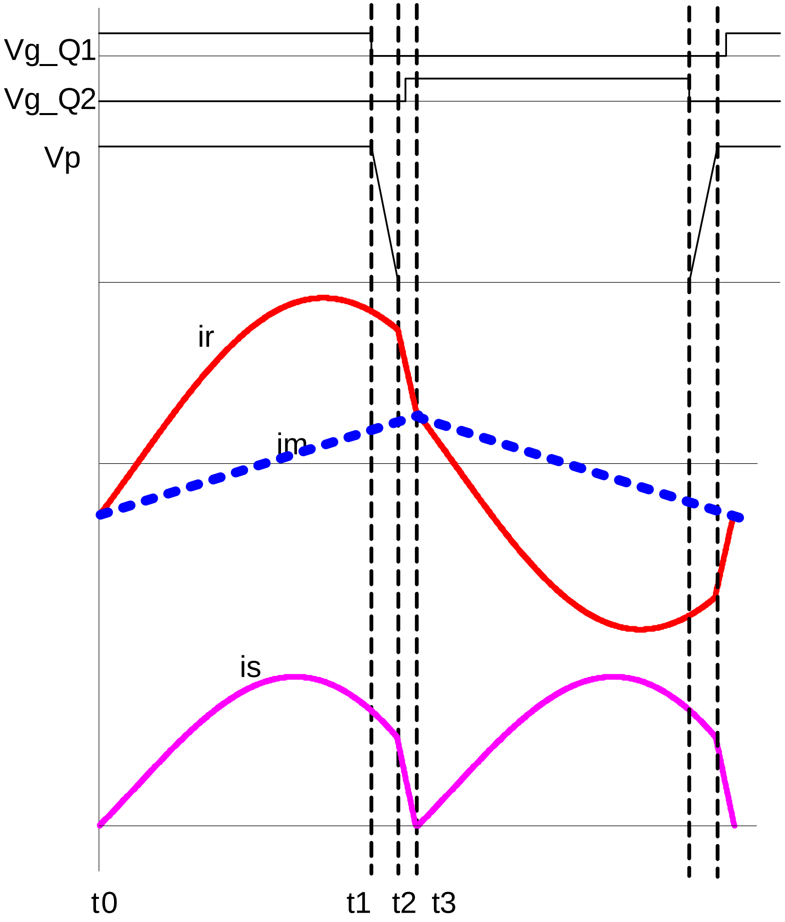


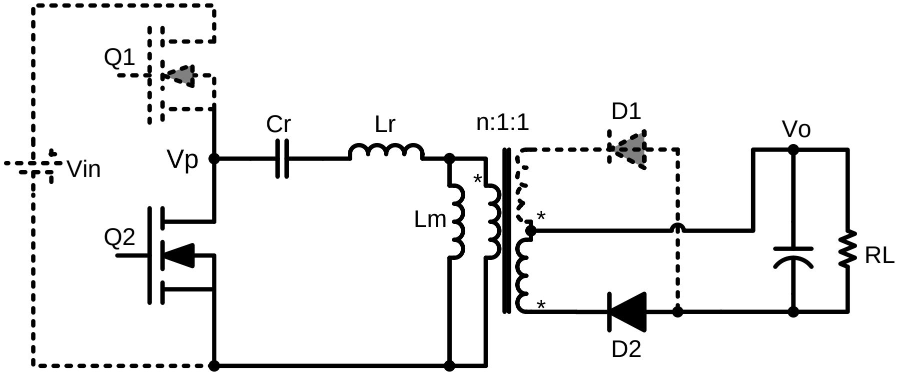


- Q2 and D2 ON, Q1 and D1 OFF
- Magnetizing current in Lm, im
- Cr resonates with Lr, ir
- Cr and Lr deliver energy to output

Operation Principle

Above Resonant Frequency

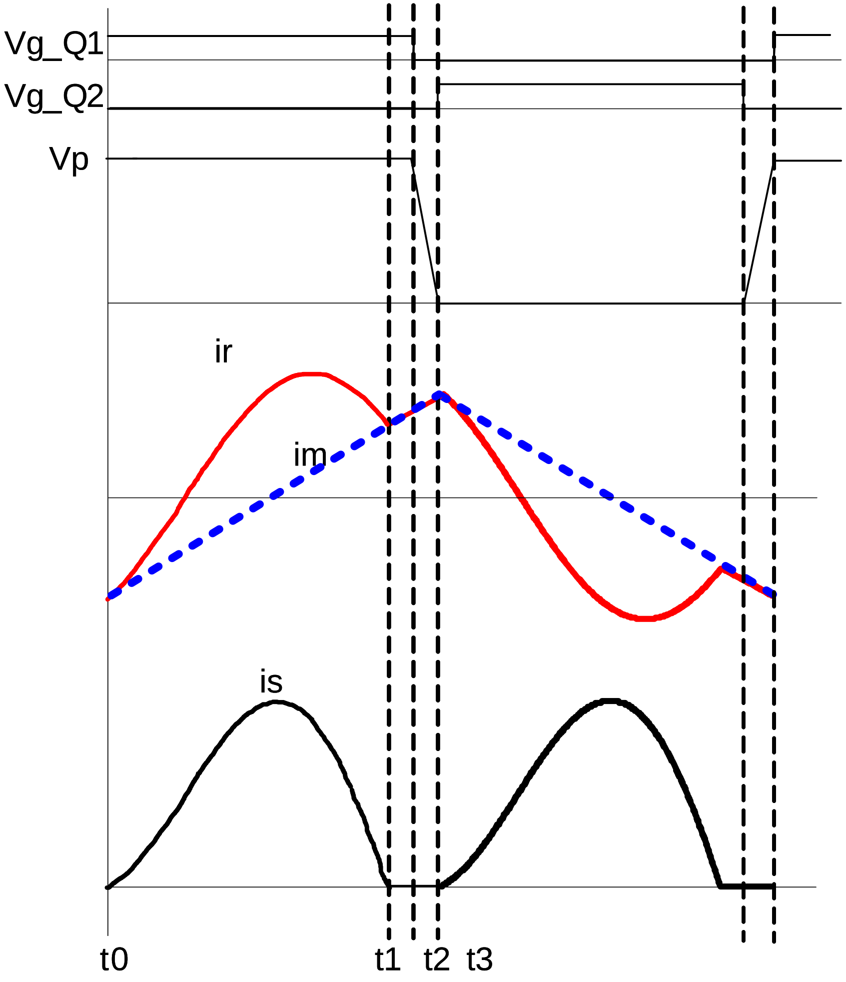


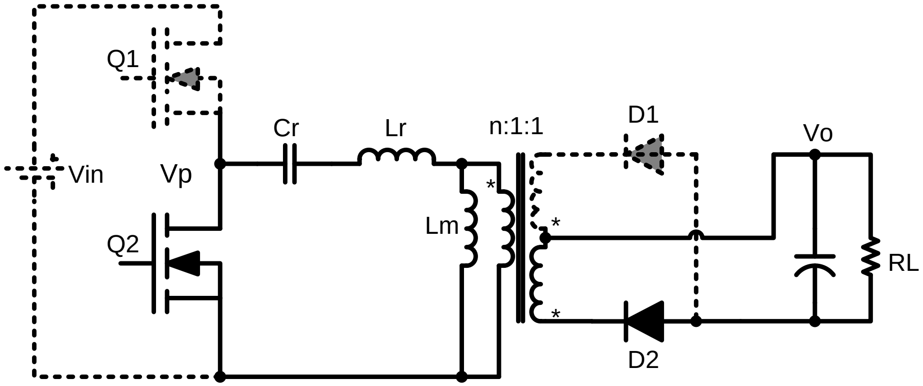


- When switching frequency is above resonant frequency, circuit behaves as SRC
- Secondary current becomes CCM, reverse recovery loss increases

Operation Principle

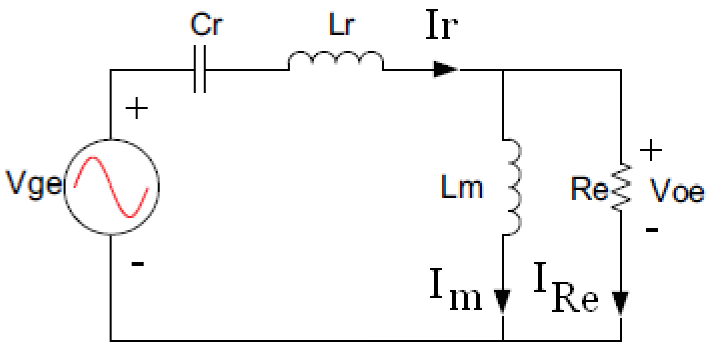
Below Resonant Frequency





- When switching frequency is below resonant frequency, magnetizing inductor begins to participate in resonant and increases voltage gain
- Secondary diode becomes discontinuous

LLC Resonant Converter Gain Function



$$M = \frac{nV_o}{V_{DC}/2} \approx$$

$$= \frac{\text{Voe}}{\text{Vge}} = \left| \frac{\dfrac{j\omega L_m R_e}{j\omega L_m + R_e}}{\dfrac{j\omega L_m R_e}{j\omega L_m + R_e} + \dfrac{1}{j\omega C_r} + j\omega L_r} \right|$$

$$V_{oe} = V_{os,1}^{rms} = \frac{2\sqrt{2}}{\pi} nV_o$$

$$R_e = \frac{8}{\pi^2} n^2 R_L$$

$$I_{\text{Re}} = I_{os,1}^{rms} = \left(\frac{\pi}{2\sqrt{2}} I_o\right)/n$$

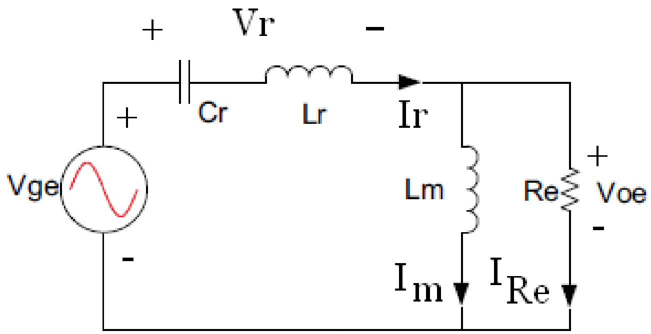
$\Downarrow$

$$M = \left| \frac{L_n f_n^2}{L_n f_n^2 + (f_n^2 - 1)(1 + j f_n L_n Q_e)} \right|$$

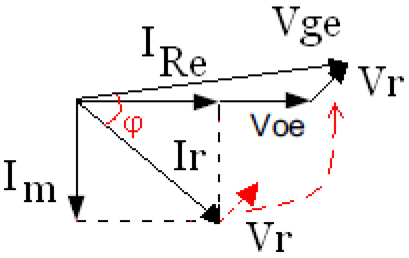
NORMALIZED GAIN	RESONANT FREQUENCY	QUALITY FACTOR	NORMALIZED FREQUENCY	INDUCTOR RATIO
$M = \dfrac{V_o}{V_{DC}/2}$	$f_0 = \dfrac{1}{2\pi\sqrt{L_r C_r}}$	$Q_e = \dfrac{\sqrt{L_r/C_r}}{R_e}$	$f_n = \dfrac{f}{f_0}$	$L_n = \dfrac{L_m}{L_r}$

LLC Resonant Converter with Wide Operation Range

- Unity gain is reached at $V_r=(V_{Lr}-V_{Cr})=0$, where input voltage in phase with output voltage, and input voltage applies to load (R_e) directly



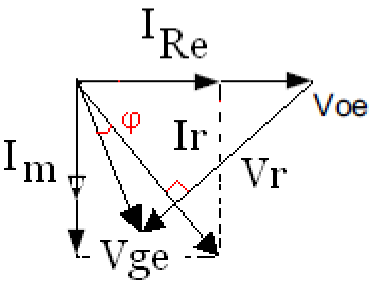
Inductive Region, Ir lagging Vge



$V_r = (V_{Lr} - V_{Cr})$

$V_{Lr} > V_{Cr}$

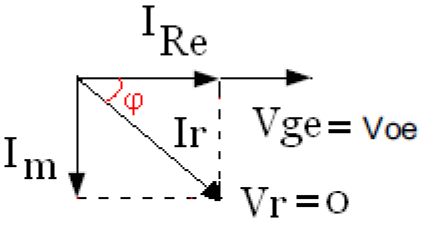
Capacitive Region, Ir leading Vge



$V_r = (V_{Lr} - V_{Cr})$

$V_{Lr} < V_{Cr}$

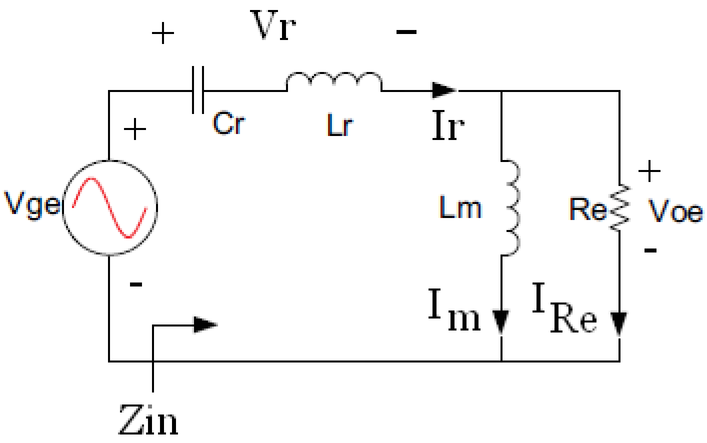
Unity Gain, Vr=0 Voe in phase with Vge

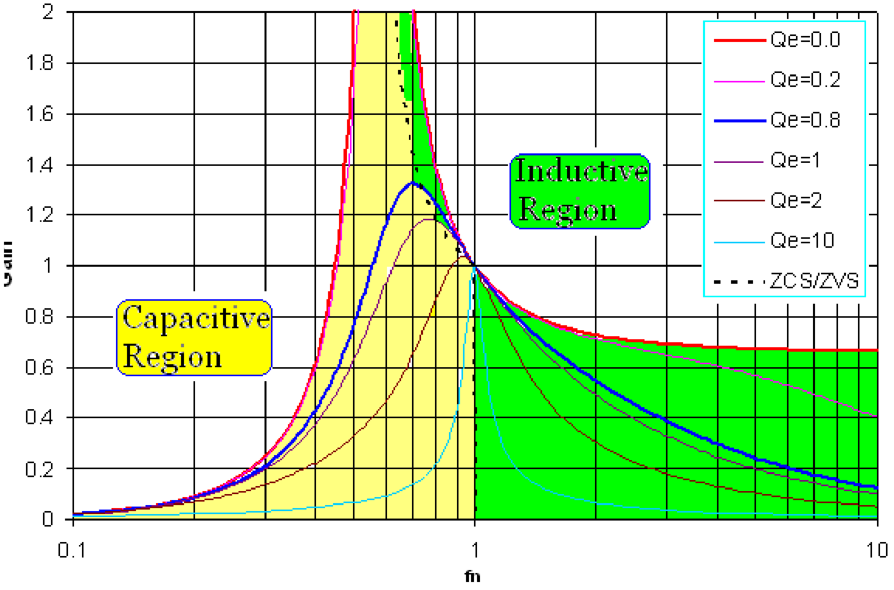


$V_r = (V_{Lr} - V_{Cr})$

$V_{Lr} = V_{Cr}$

LLC Resonant Converter with Wide Operation Range





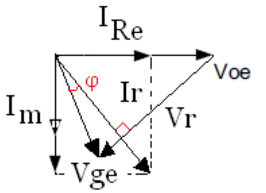
Working regions (Modes)

- Inductive Region, if resonant network current is lagging input voltage
- Capacitive Region, if resonant network current is leading input voltage
- Resistive Region, if resonant network current is in phase with input voltage (boundary to divide Inductive and capacitive, by let the imaginary part zero of the input impedance)
- Unity gain happens at (V_{Lr}-V_{Cr})=0, where input voltage in phase with output voltage, and input voltage applies to load (R_e) directly

LLC Resonant Converter with Wide Operation Range

- Should operate in ZVS region (Inductive Region, I_r lagging Vge)

- Avoid ZCS region (Capacitive Region, I_r leading Vge)
  - – Hard switching of half bridge switches
  - – Reverse recovery losses in primary FET body diodes
  - – Large spikes on switch node
  - – Higher EMI levels
  - – Frequency relationship reversed
    - Frequency increases as load increases



$V_r = (V_{Lr} - V_{Cr})$

$V_{Lr} < V_{Cr}$

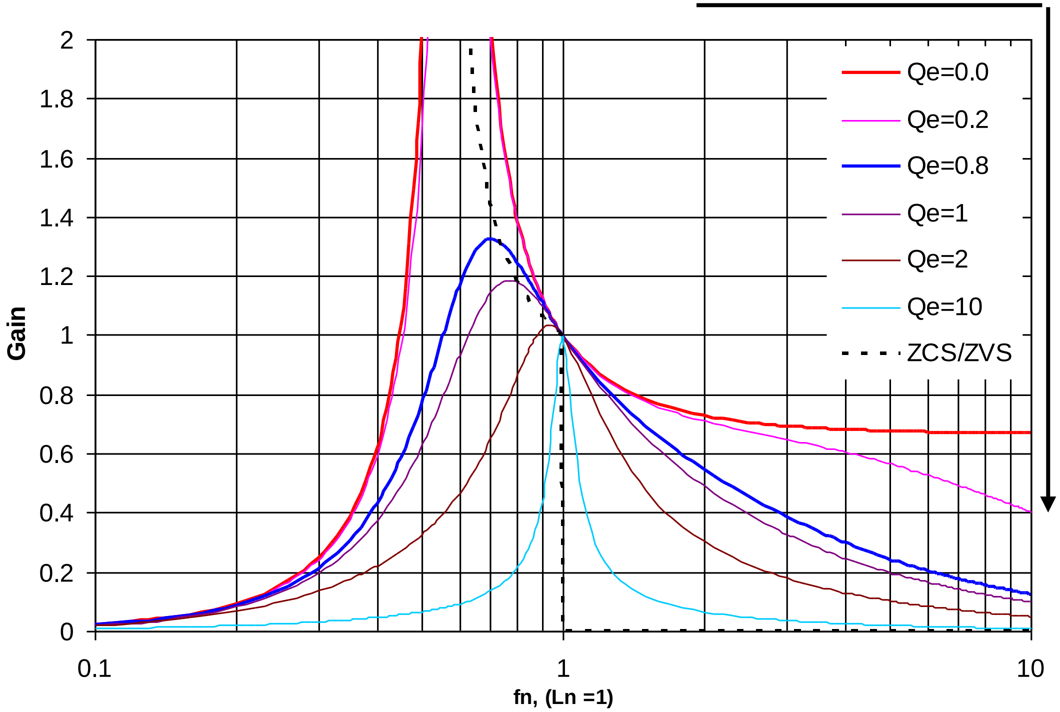
Gain Characteristics with Ln and Qe

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e}$$

Q_e is related to output load

Q_e Increasing with Load Current

$$R_e = \frac{8}{\pi^2} n^2 R_L$$



$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$$

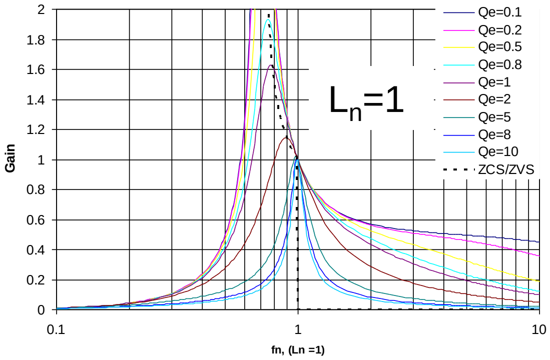
$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$$

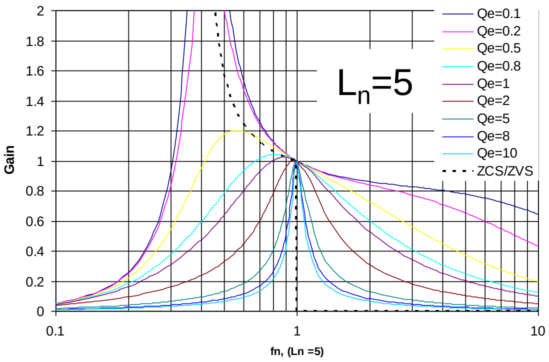
$$f_n = \frac{f}{f_0}$$

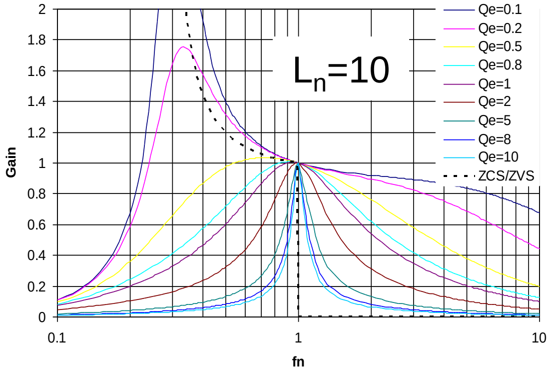
Qe increase with Ln constant (designed Lr, Cr, and operational RL),

- Peak-gain becomes lower
- Frequency at peak-gain moving to right
- Better “frequency-selective

Impacts of Circuit Parameters





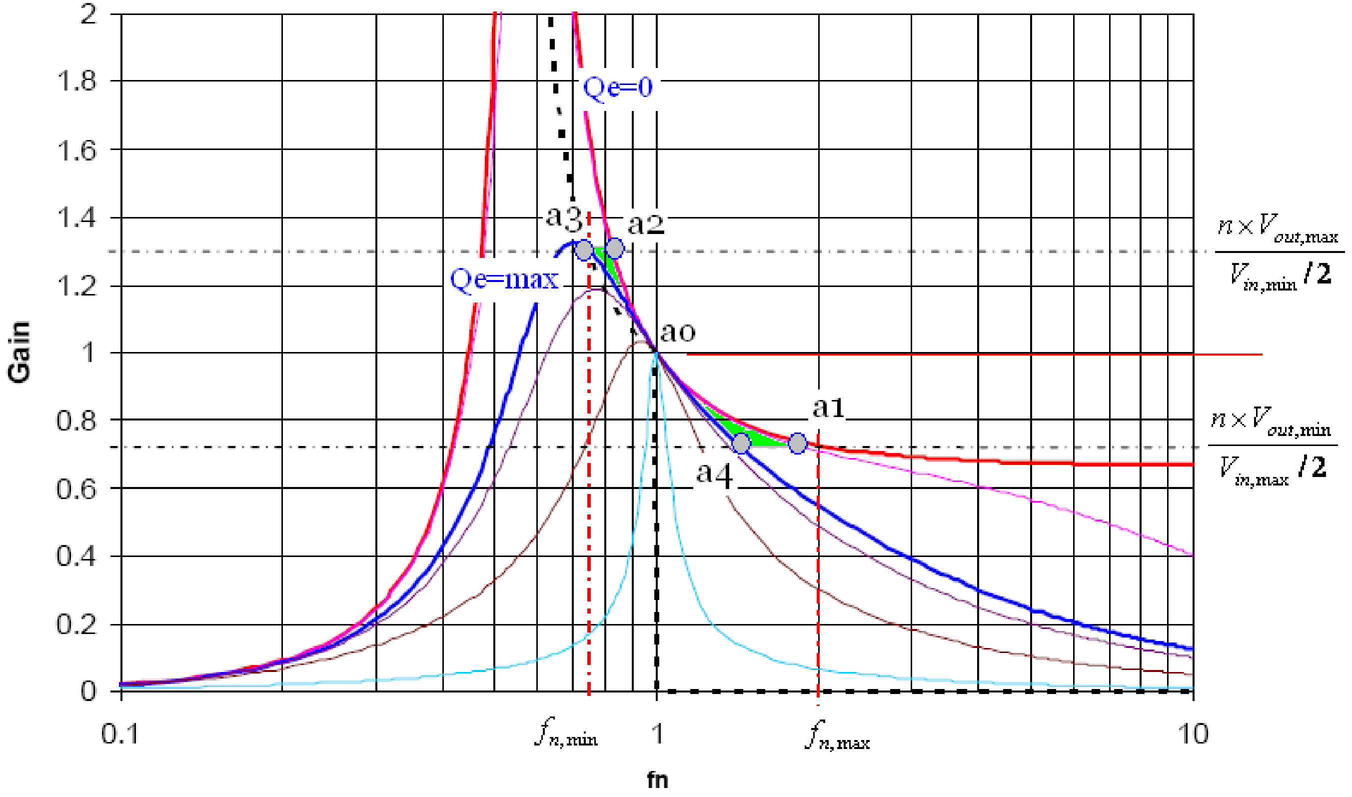


Gain Change with Ln and Qe

- Ln increase with Qe constant (designed Lr, Cr, and operational RL),
  - flat,
  - magnitude shift-up,
  - frequency value at peak-gain moving towards more left,
  - less “frequency-selective”
  - wide frequency variation from no load to full load (more discussion later)

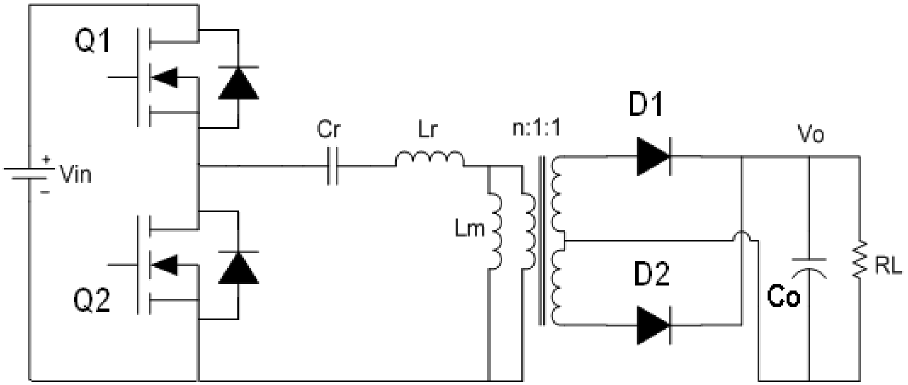
Ln somewhere 3 to 5 look best balance between peak gain and frequency change – can be initially pick-up

LLC Resonant Converter Operation for design consideration



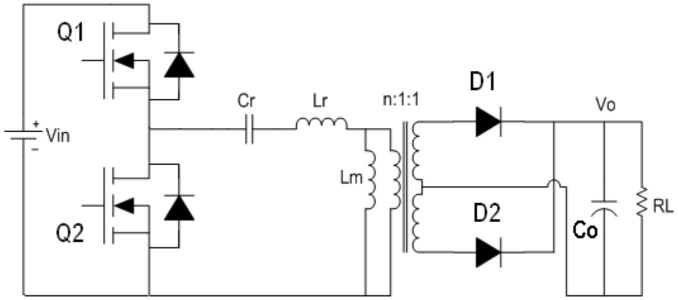
- Operation/design with no load and minimum gain at a1
- Operation /design with full load and maximum gain at a3
- All gain curves cross at unity at f_n=1, or f=f_0
- Qe design consideration at Heavy load, OCP, Short Circuit

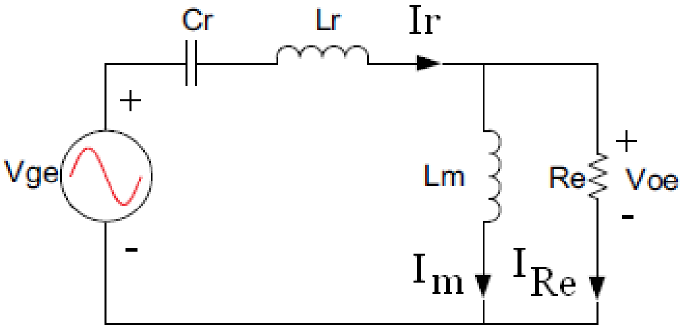
Design Goals for LLC Resonant Converter

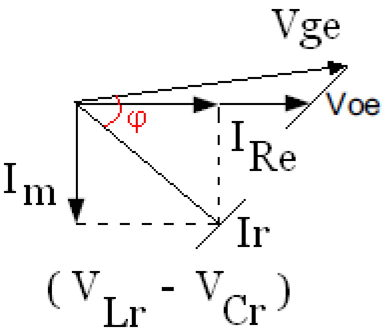


- Minimize RMS current under normal operation condition
- Ensure ZVS operation
- Ensure desired operation range

Design Consideration -1: *Primary RMS Current at Normal Operation*





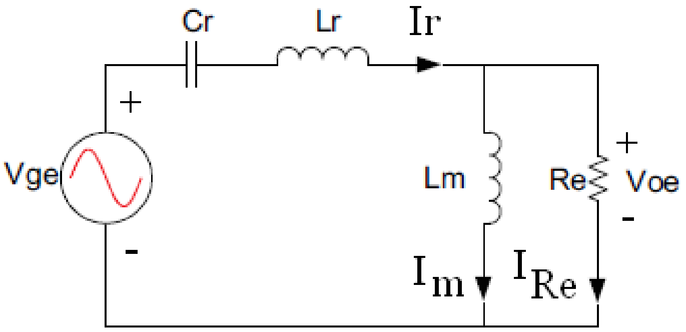


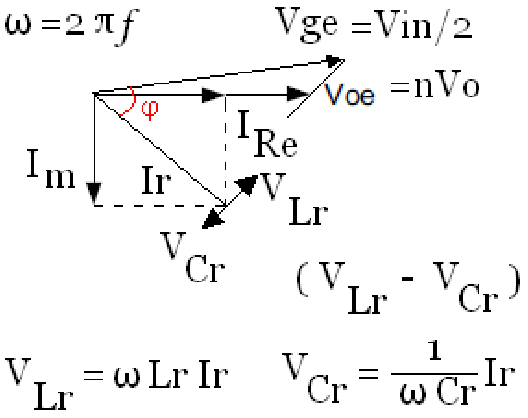
$$I_{P,RMS} = I_r = \sqrt{I_m^2 + I_{\mathrm{Re}}^2} =$$

$$FHA \rightarrow \sqrt{\left(\frac{2\sqrt{2}}{\pi}\frac{nV_O}{\boxed{\omega L_m}}\right)^2 + \left(\frac{\pi}{2\sqrt{2}}\frac{I_o}{n}\right)^2}$$

- Primary current can be easily calculated from the phasor circuit
- Primary side RMS current is summation of magnetizing current and load current
- Larger Lm is better for less conduction losses

Design Consideration -2: *Secondary winding RMS Current*



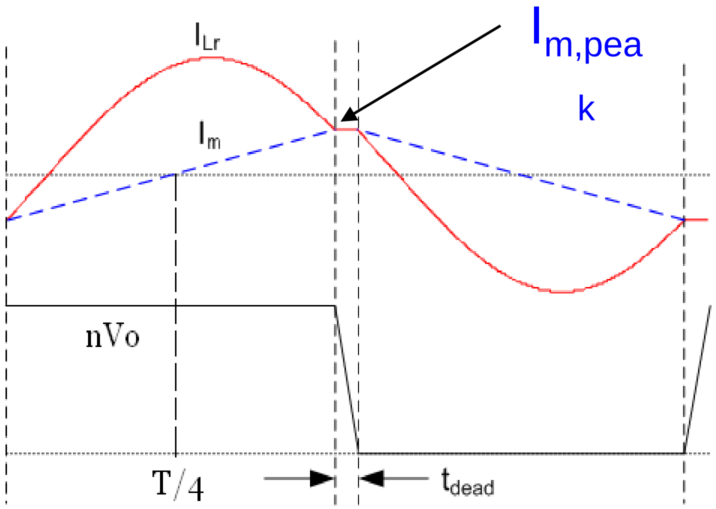


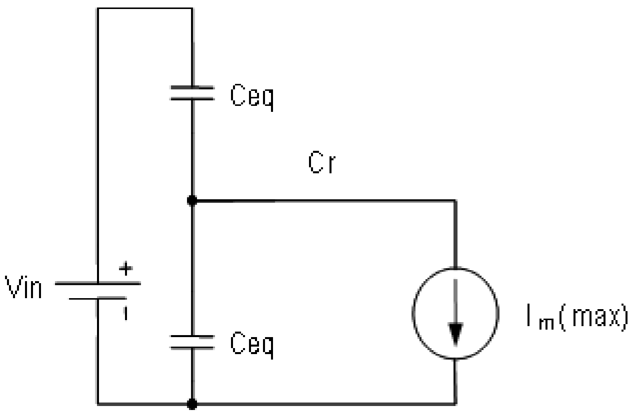
$$I_{RMS\_S} = (I_{\text{Re}} \times n)/2 = \frac{\pi}{4\sqrt{2}} I_o \Rightarrow I_{peak\_S} = \frac{\pi}{4} I_O, \quad center - tapped$$

$$I_{RMS\_S} = I_{\text{Re}} \times n = \frac{\pi}{2\sqrt{2}} I_o \Rightarrow I_{peak\_S} = \frac{\pi}{2} I_O, \qquad bridge$$

- Secondary side current is the difference between resonant tank current and magnetizing current

Design Consideration -3: *Zero Voltage Switching*





$$I_{m,peak} = \frac{nV_o}{L_m}\frac{T}{4}$$

$$\frac{1}{2}(L_m + L_r)I_{m,peak}^2 \geq \frac{1}{2}(2C_{eq})V_{in}^2$$

$$I_{m,peak} \times t_{dead} \geq 2C_{eq}V_{in}$$

$$L_m \leq \frac{T \times t_{dead}}{16C_{eq}}$$

ZVS conditions:

- Enough H-field energy to balance E-field Energy in less than half cycle
- Enough time to make the energy conversion
- Worst operation for ZVS,
  - $V_{o,min}$, $I_{m,peak}$ becomes small
  - $V_{in,max}$, more C_{eq} energy needs to discharge

Trade-off Design of Dead Time

$L_m \uparrow \Rightarrow t_{dead} \uparrow$

- Smaller turn off current
- Smaller magnetizing current

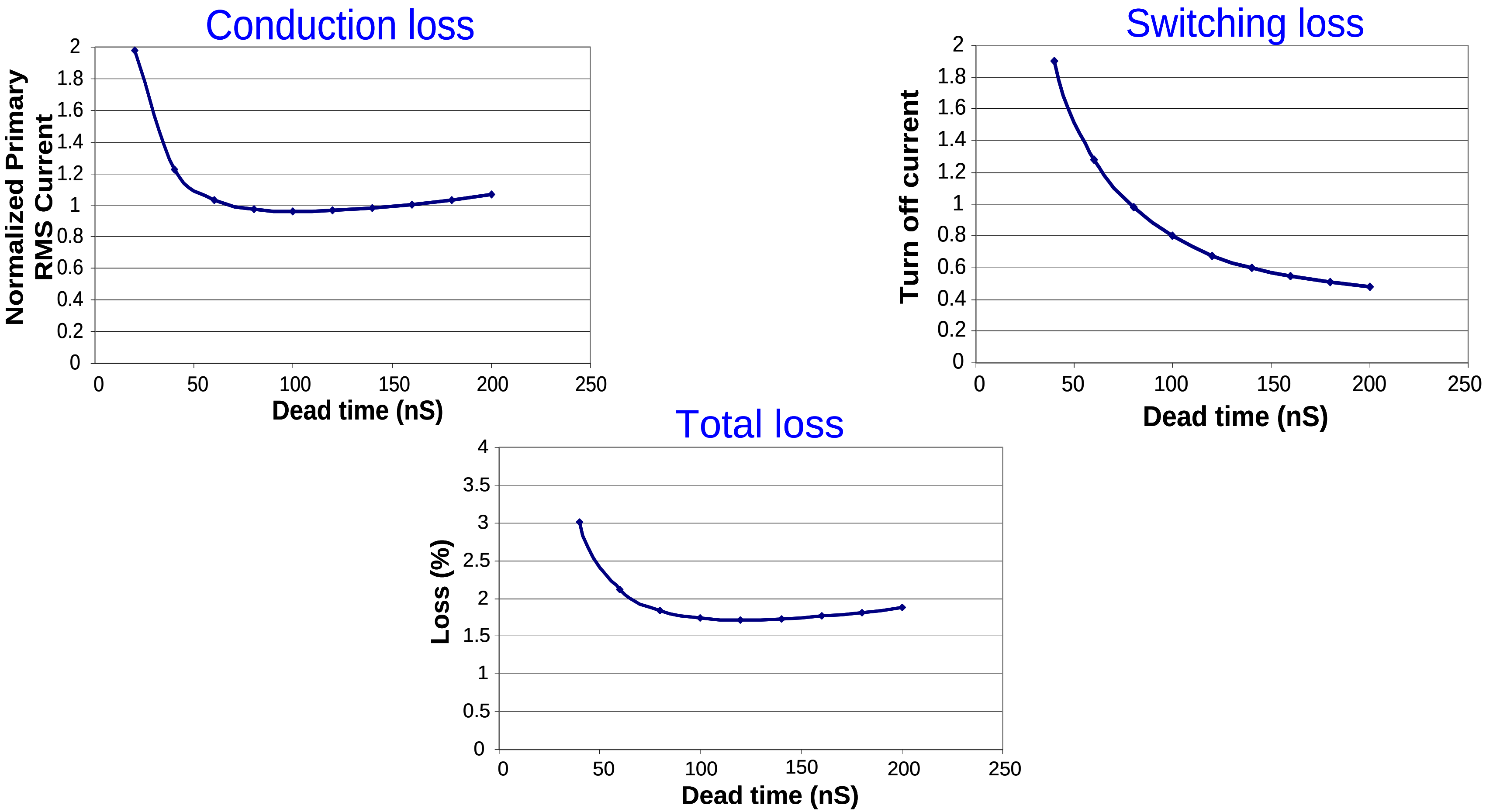
- Increase RMS current due to duty cycle loss

$L_m \downarrow \Rightarrow t_{dead} \downarrow$

- Smaller duty cycle loss

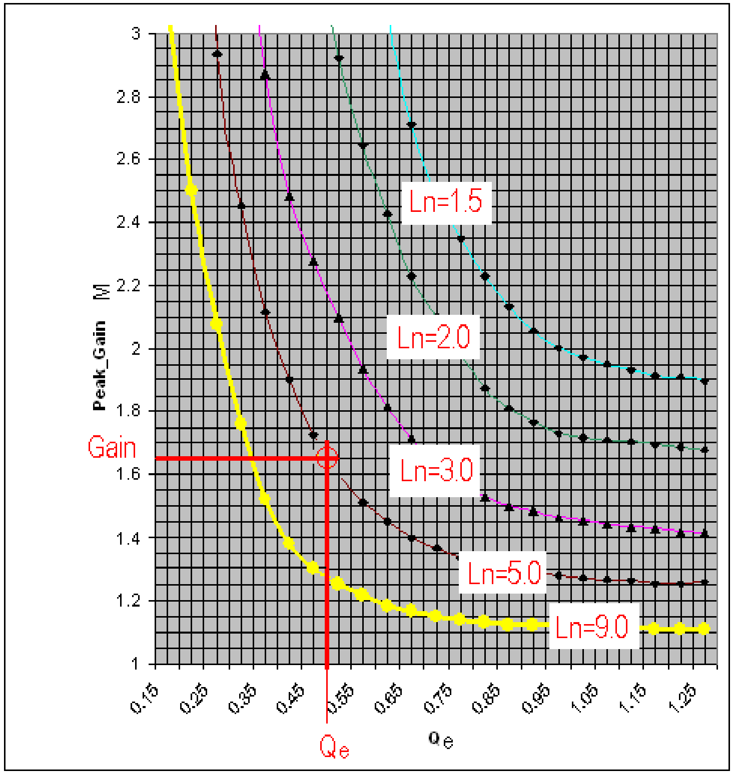
- Larger magnetizing current
- Larger turn off loss

Trade-off Design of Dead Time



- ➢ Trade-off between the switching loss and conduction loss on a case of 100ns dead time

Peak Gains with Ln and Qe



- ➢ Initially select Ln in the range of 3 to 5 (gain curve not very flat and able to narrow down the frequency change while there is still enough gain)
- ➢ Find proper Qe to get enough peak gain

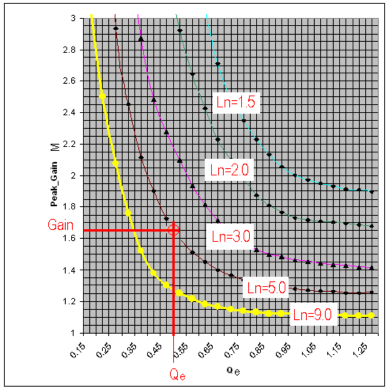
Design Flow Chart for LLC Resonant Converter

Converter Specifications

$$n = \frac{V_{in}}{2V_O}$$

choose an L_n and Q_e

Check max gain against graph



Peak gain enough?

No

Change L_n and Q_e

Yes

Calculate Re

$$R_e = \frac{8}{\pi^2} n^2 R_L = \frac{8n^2 V_o^{\,2}}{\pi^2 P_{out}}$$

Resonant Capacitor

$$C_r = \frac{1}{2\pi Q_e R_e f_{sw}}$$

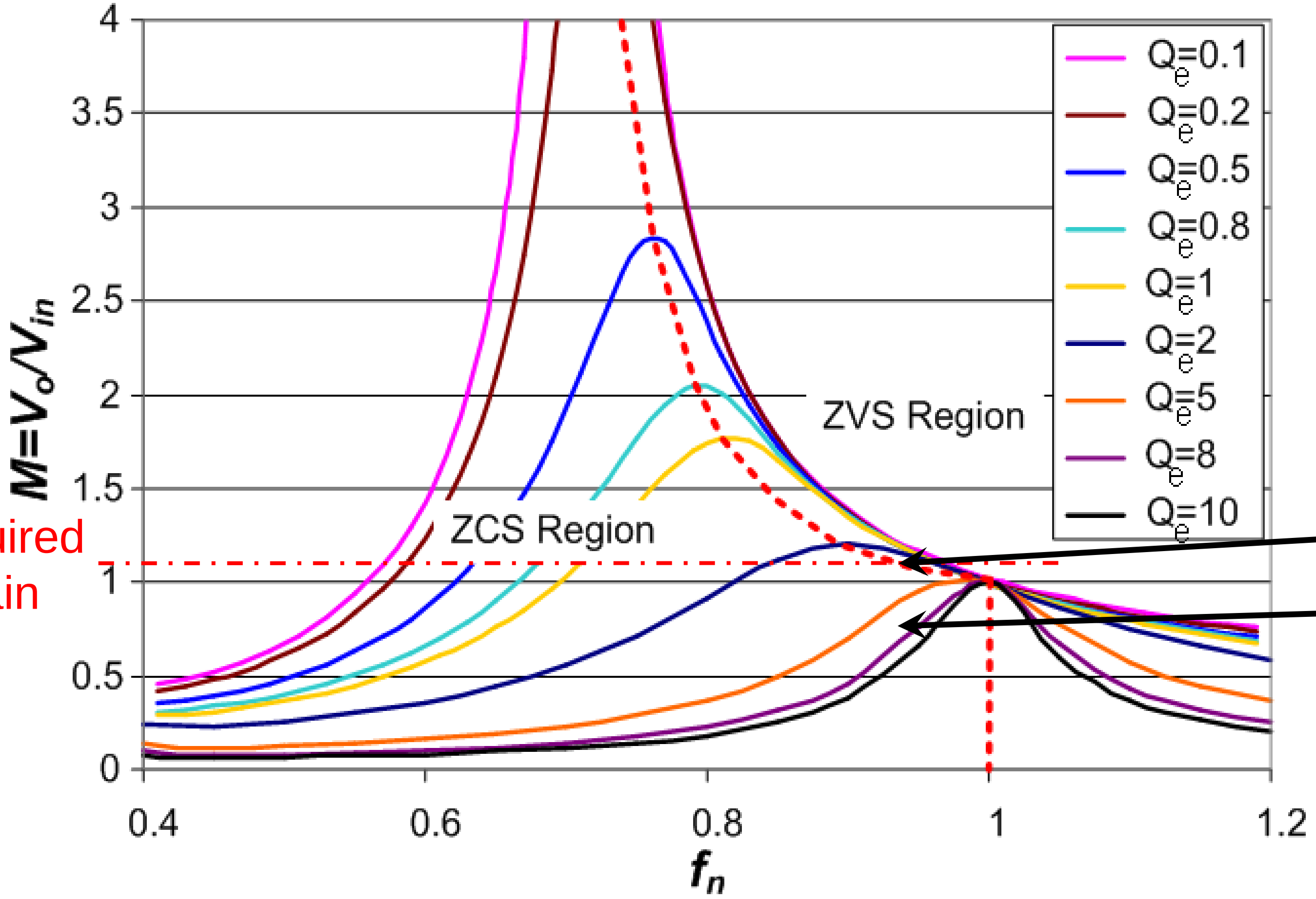
Resonant Inductor

$$L_r = \frac{1}{(2\pi f_{sw})^2 C_r}$$

Magnetizing Inductance

$$L_m = L_n L_r$$

Design - *Over Current Protection*



$$Q_e = \frac{\sqrt{Lr/Cr}}{R_e}$$

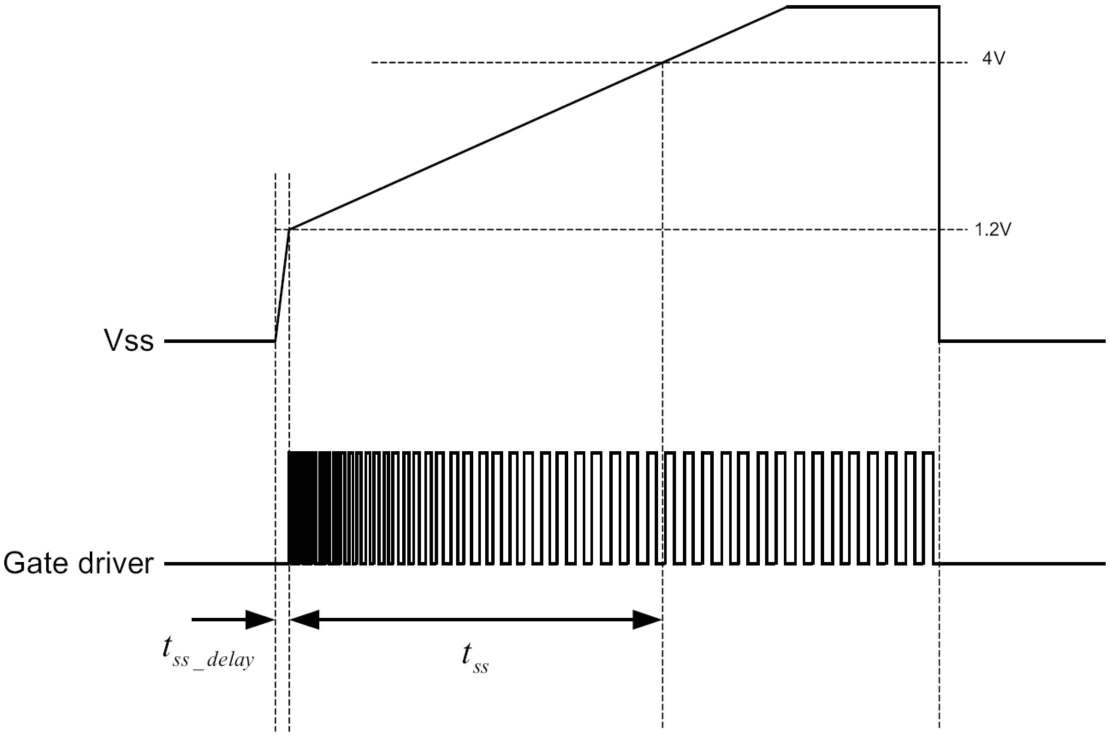
Required Gain

Max load

Overload?

- ➢ During over load condition, check if the converter enters ZCS region

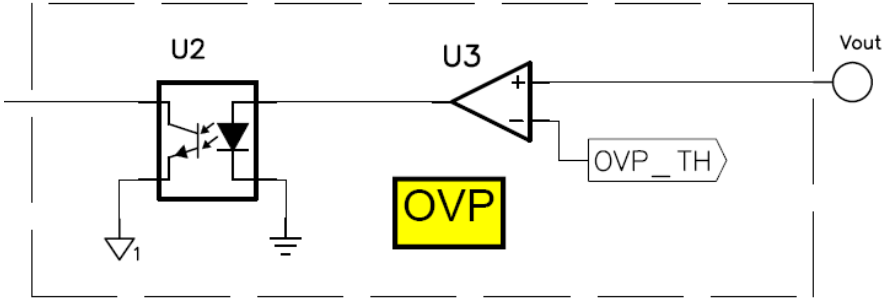
Design - *Soft start*



- Soft start is achieved by frequency control

Design – *OVP and Burst Operation*

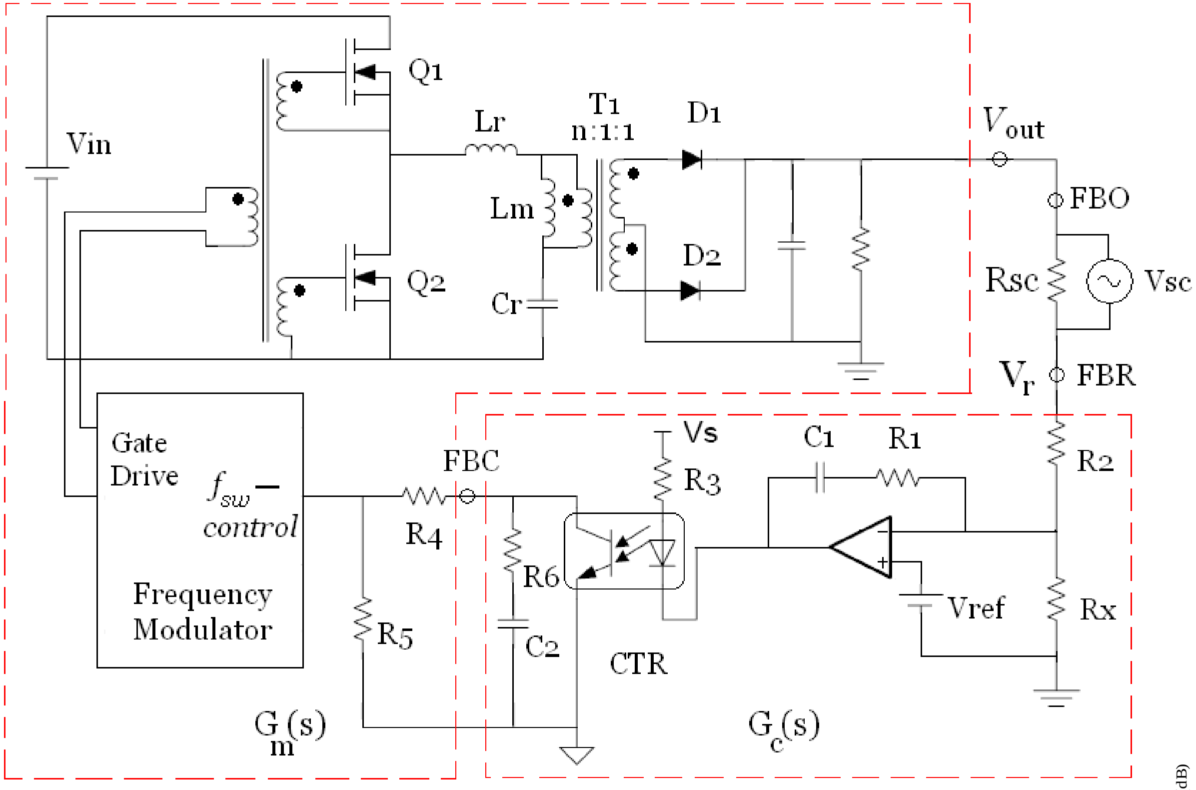
- Secondary OVP
  - Feedback loop fault may cause output over voltage.
  - Slow loop response may also cause OVP.
  - Independent OVP circuit is needed.

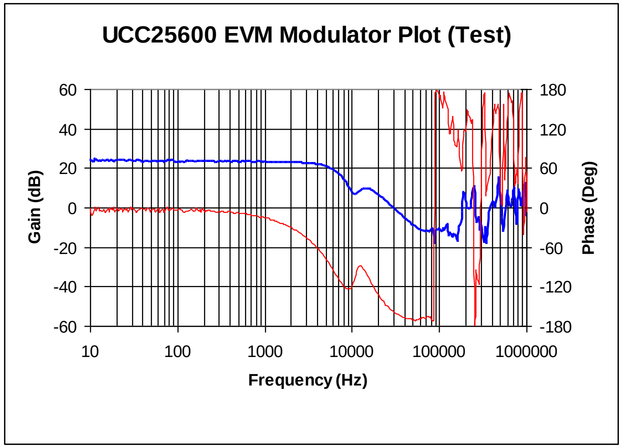


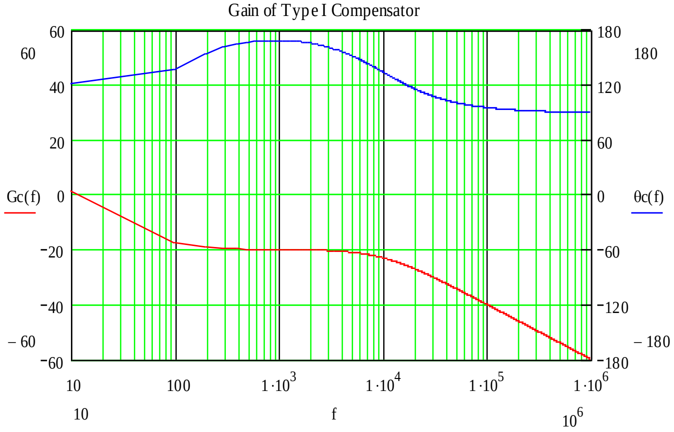
- Burst Operation
  - To cover no load operation, smaller Ln is needed which increases circulating (magnetizing) current, leading more conduction losses.
  - To reduce switching losses, ZVS is still needed at no load. This requires higher magnetizing current, too.
  - To maintain output regulation, burst operation at light load and no load is an alternative to balance switching losses and conduction losses.

Feedback Loop Design

$$G_c(S) = K_{dc}\frac{\frac{S}{C1\times R2}+1}{S\times\left(\frac{k_{opto}S}{2\pi\times f_{p\_opto}}+1\right)}$$





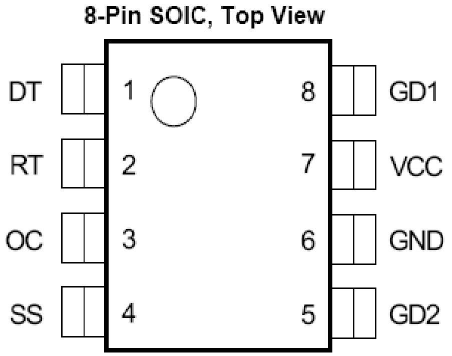


- Measure $G_m(j\omega)$
- Design $G_c(j\omega)$ based on $G_m(j\omega)$ measurement

Summary

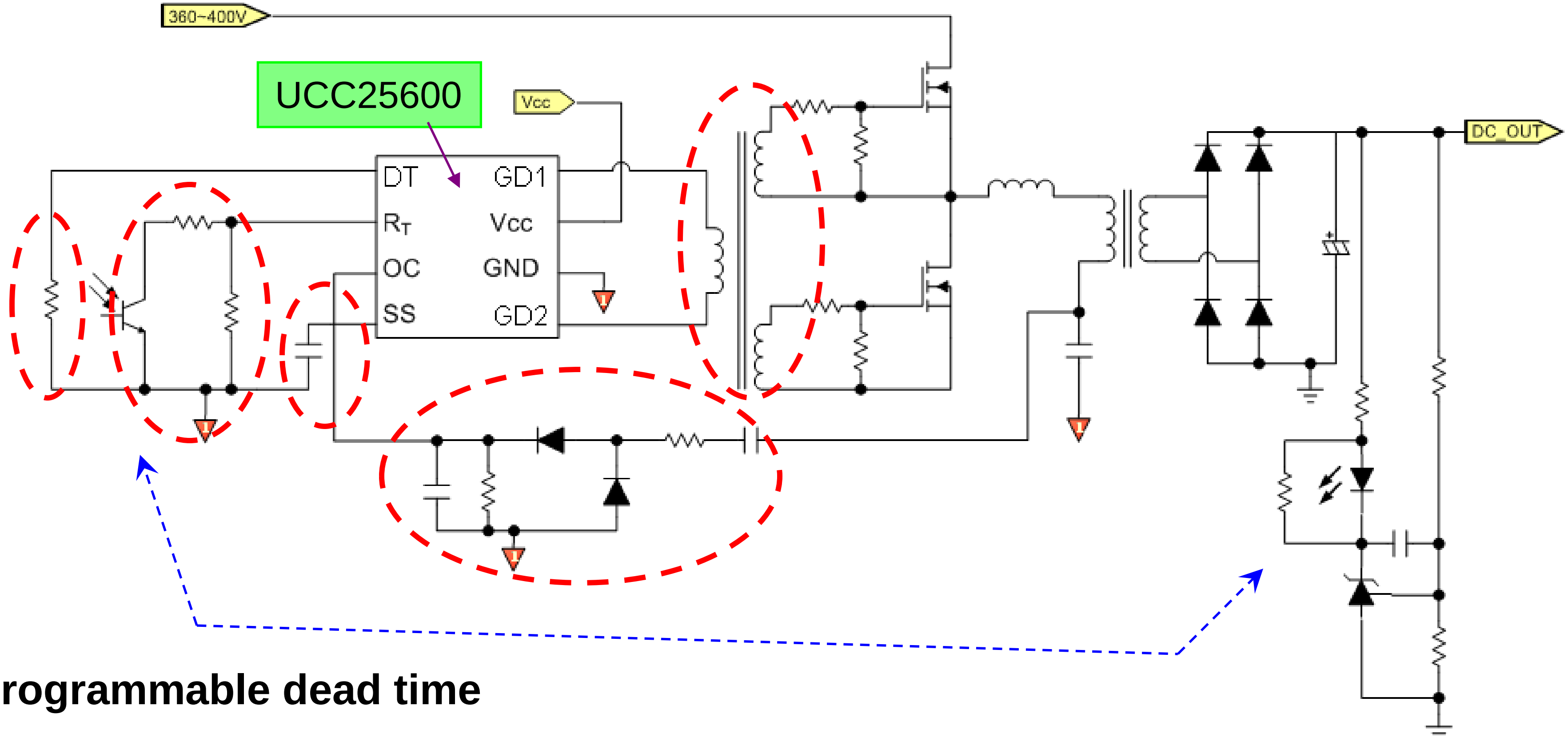
- LLC resonant converter is able to achieve wide operation together with high efficiency
- Due to low switching losses, LLC resonant converter is able to operate at high switching frequencies, while maintaining high efficiency
- LLC resonant converter design needs to find a suitable magnetizing inductor to ensure small conduction losses and switching losses
- By choosing a suitable Ln and Qe value, desired voltage gain can be achieved to input and output voltage variation range

UCC25600 Resonant Half Bridge Controller



- Complete system features
  - Programmable soft start
  - Programmable dead time
  - Programmable maximum/minimum switching frequency
  - 0.4A source, 0.8A sink driving capability
  - Simple ON/OFF control
  - Burst operation at light load condition
- Precise timing control
  - 3% accuracy on minimum switching frequency setting with only external resistor
  - ±50ns matching on dead time
  - Soft start timer range from 1ms to 500ms
- Complete protection functions
  - Two levels over current protection, auto recovery and latch off
  - Bias voltage UVLO and OV protection
  - Over temperature protection
  - Soft start enabled after all fault conditions
- 8 pin SOIC package, simplifies design and layout

Application Circuit



Programmable dead time

Frequency control with minimum/maximum frequency limiting

Programmable soft start with on/off control

Two level over current protection, auto-recovery and latch up

Matching output with 50ns tolerance

Test based on EVM (UCC25600EVM)

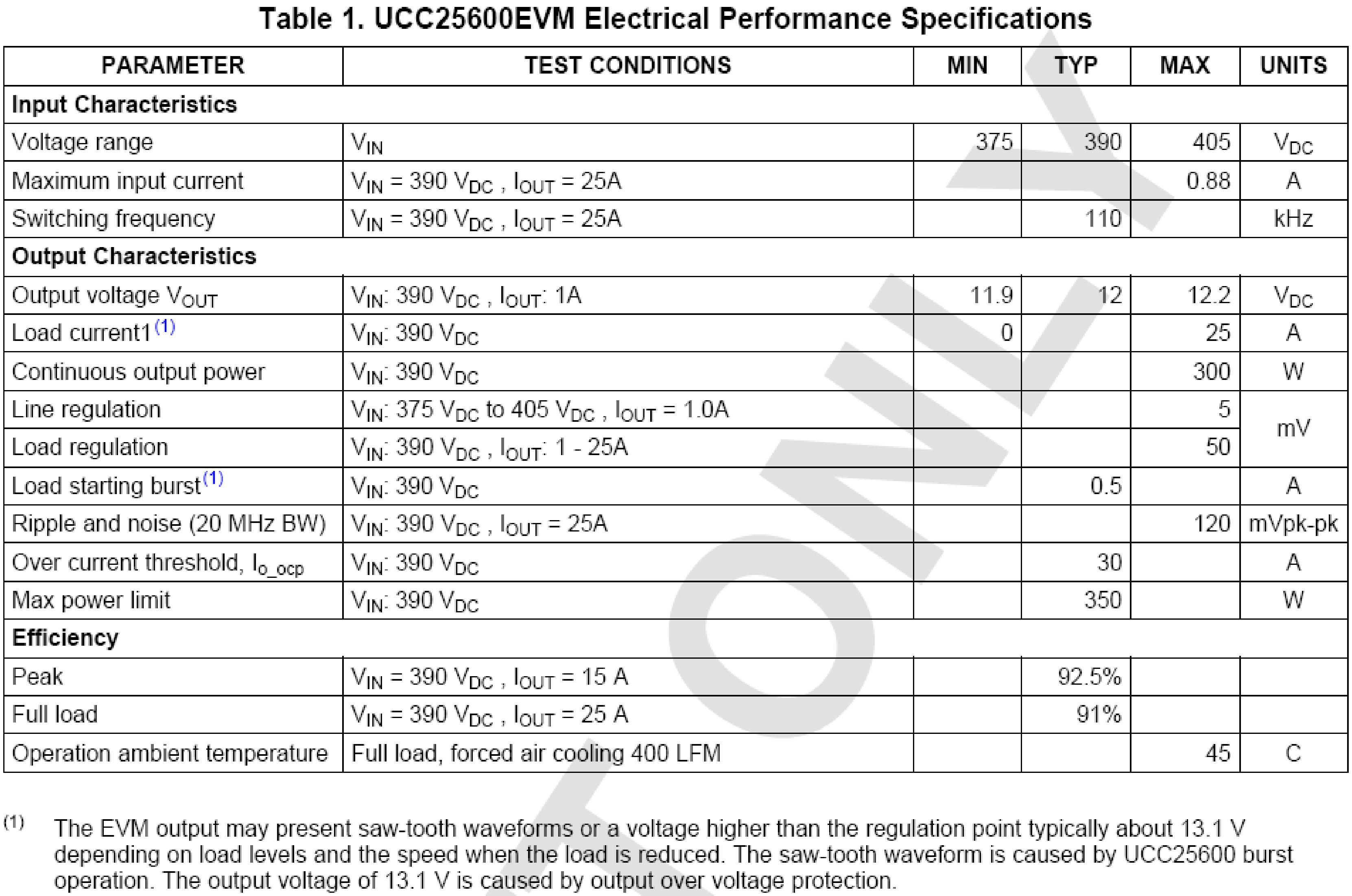


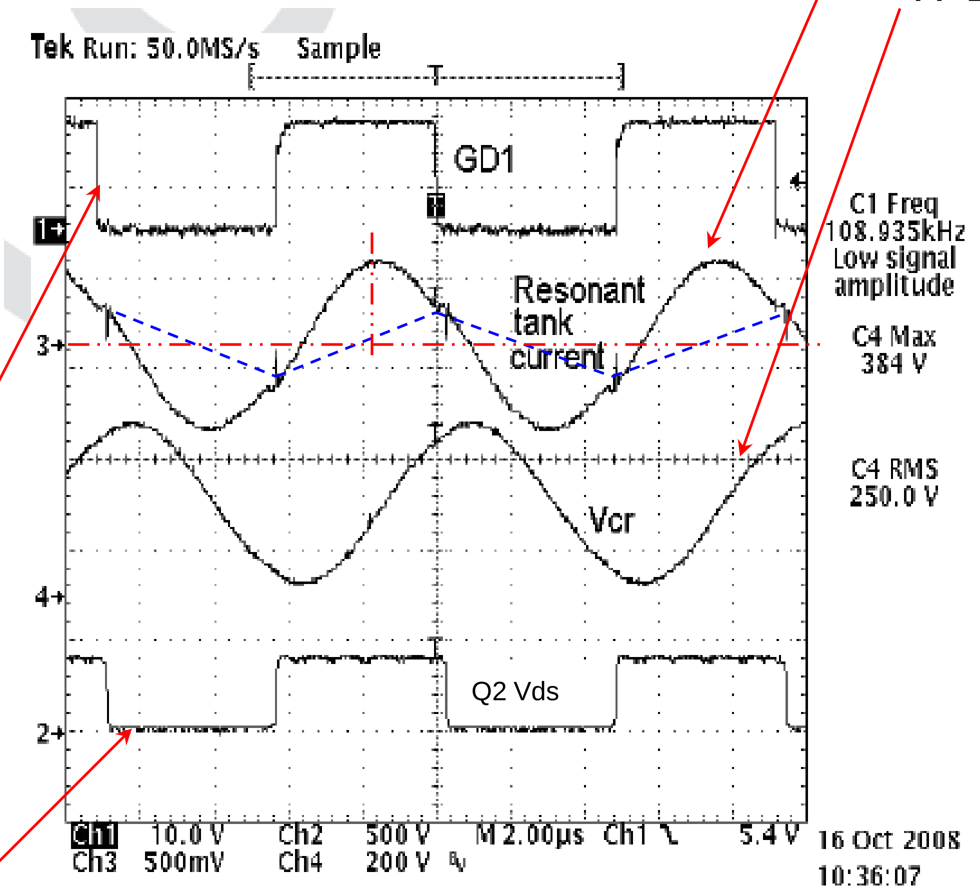
Table 1. UCC25600EVM Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range	V_{IN}	375	390	405	V_{DC}
Maximum input current	$V_{IN} = 390\ V_{DC}$, $I_{OUT} = 25A$			0.88	A
Switching frequency	$V_{IN} = 390\ V_{DC}$, $I_{OUT} = 25A$		110		kHz
Output Characteristics					
Output voltage V_{OUT}	V_{IN}: 390 V_{DC}, I_{OUT}: 1A	11.9	12	12.2	V_{DC}
Load current1(1)	V_{IN}: 390 V_{DC}	0		25	A
Continuous output power	V_{IN}: 390 V_{DC}			300	W
Line regulation	V_{IN}: 375 V_{DC} to 405 V_{DC}, $I_{OUT} = 1.0A$			5	mV
Load regulation	V_{IN}: 390 V_{DC}, I_{OUT}: 1 - 25A			50	
Load starting burst(1)	V_{IN}: 390 V_{DC}		0.5		A
Ripple and noise (20 MHz BW)	V_{IN}: 390 V_{DC}, $I_{OUT} = 25A$			120	mVpk-pk
Over current threshold, I_{o_ocp}	V_{IN}: 390 V_{DC}		30		A
Max power limit	V_{IN}: 390 V_{DC}		350		W
Efficiency					
Peak	$V_{IN} = 390\ V_{DC}$, $I_{OUT} = 15\ A$		92.5%		
Full load	$V_{IN} = 390\ V_{DC}$, $I_{OUT} = 25\ A$		91%		
Operation ambient temperature	Full load, forced air cooling 400 LFM			45	C

(1) The EVM output may present saw-tooth waveforms or a voltage higher than the regulation point typically about 13.1 V depending on load levels and the speed when the load is reduced. The saw-tooth waveform is caused by UCC25600 burst operation. The output voltage of 13.1 V is caused by output over voltage protection.

Test with EVM: Resonant Tank

- Ch3: Lr Current
  - Scale: 3.4A/div
- Primary Peak Current: 2.72A
- Secondary Peak Current (Nt=16.7):
  - 3.4A/div x 0.8div x 16.7 = 45.4A
- Load Current: 25A
  - Io/Is = 25/45.4 =0.55
  - Compare: half wave rectifier



TP2

TP13

TP24

TP6

Figure 11. Typical Resonant Tank Current and Resonant Capacitor Voltage

Test with EVM: Ripple and Hiccup

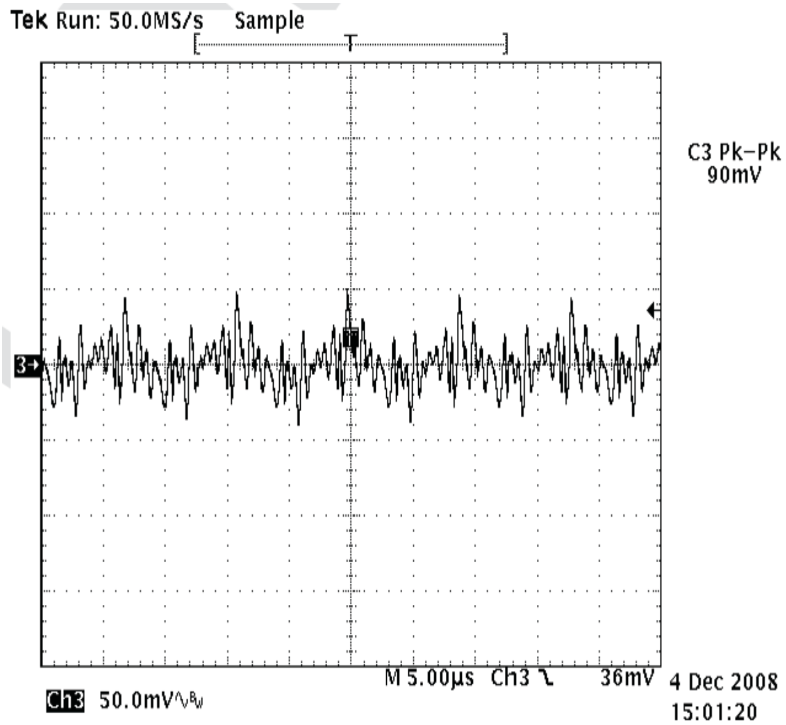
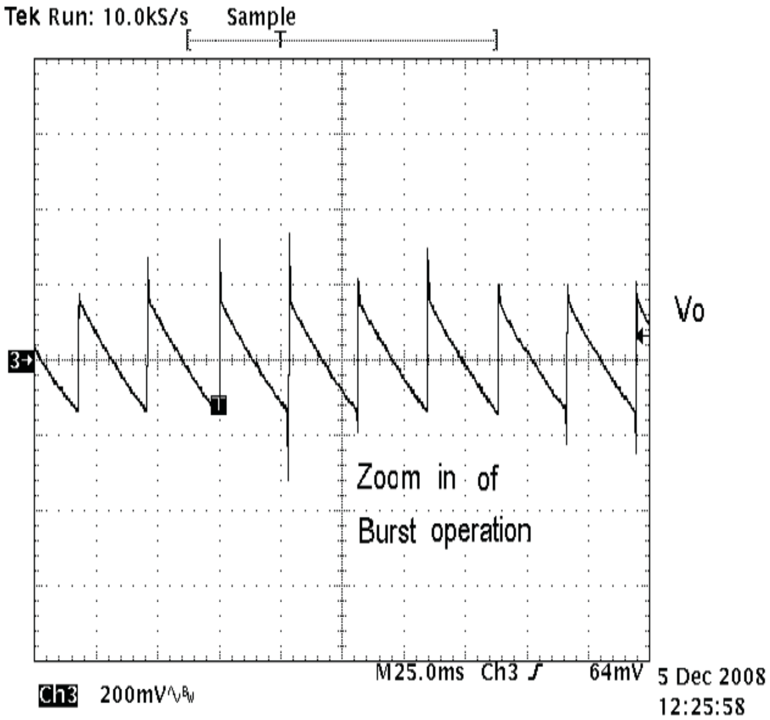


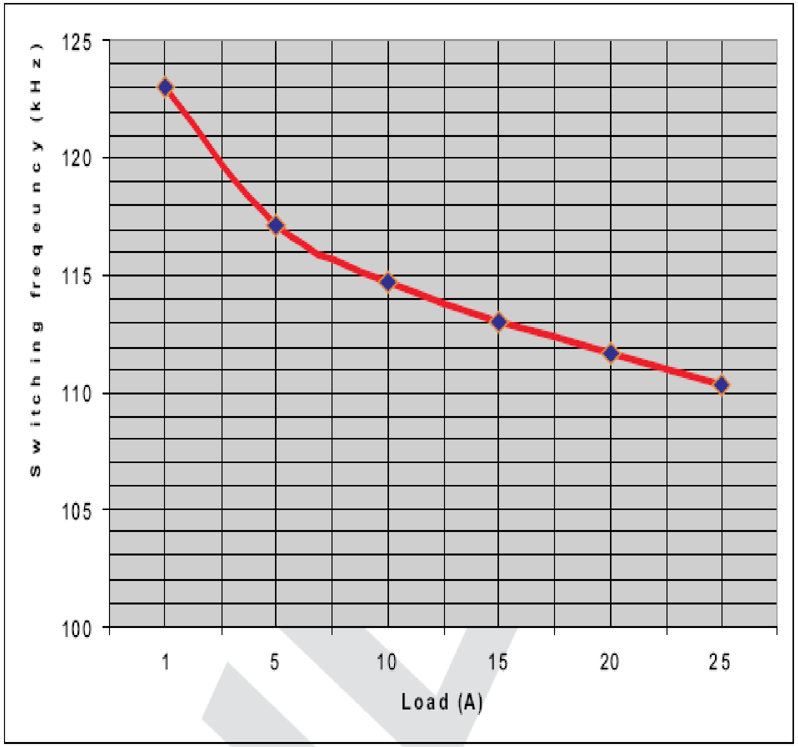
Figure 7. Typical Output Voltage Ripple Waveform at V_{IN} = 390 V and I_O = 15 A (TP15)

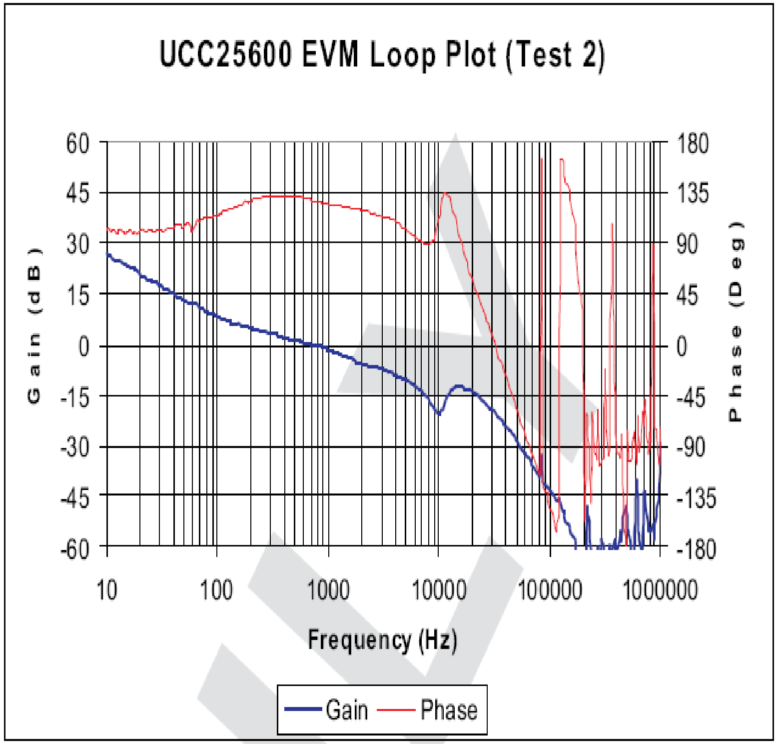


Zoom in of Burst operation

Figure 16. Typical Output Voltage in Burst Operation (TP15)

Test with EVM: Freq and Feedback

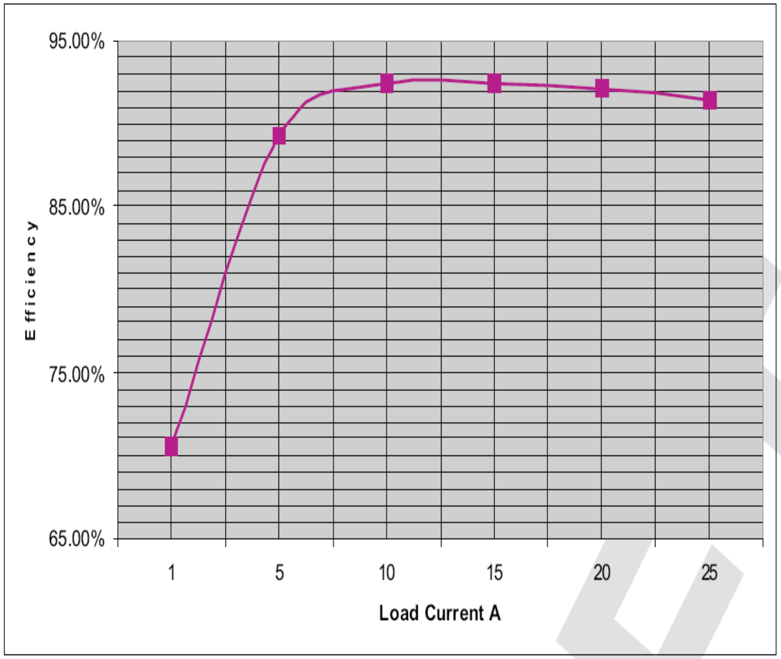




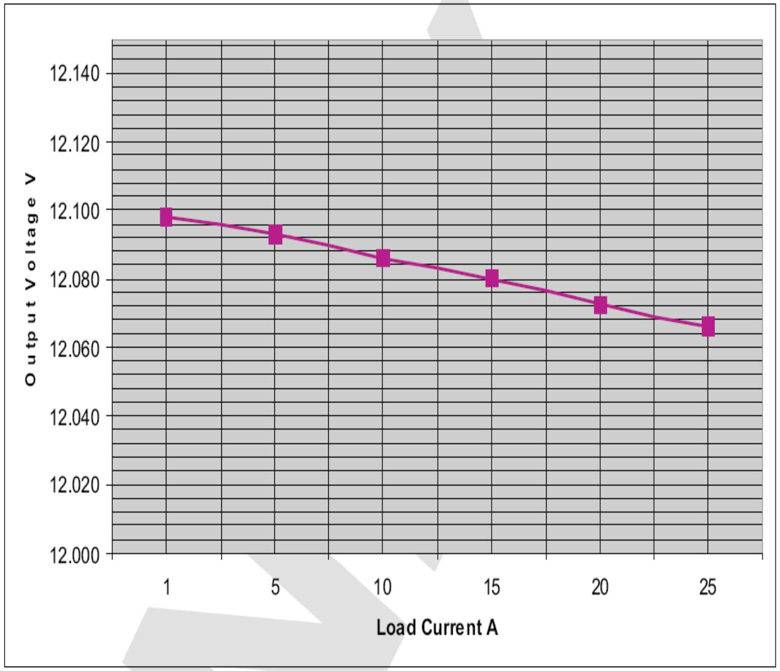
Frequency Variation

Feedback Loop Bode Plots

Test with EVM: Efficiency and Load Regulation



Efficiency



Load Regulation

Thank You!